REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-22 in the application. No claims have been cancelled or added. In the present response, the Applicants have amended Claims 1, 8 and 15. Accordingly, Claims 1-22 are currently pending in the application.

I.   Rejection of Claims 1-22 under 35 U.S.C. §112

The Examiner rejected Claims 1-22 under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. In particular, the Examiner has stated that the claimed meaning of "background task" is indefinite since there are no grouping of tasks to give meaning to "background task." (Examiner's Action, page 2). In response, the Applicants have amended independent Claims 1, 8 and 15 to reflect a grouping of a plurality of tasks into foreground and background tasks. Accordingly, the Applicants respectfully request the Examiner to withdraw the rejection under 35 U.S.C. §112, second paragraph, with respect to independent Claims 1, 8 and 15 and Claims dependent thereon.

II.   Rejection of Claims 1, 4, 7, 8, 11 and 14 under 35 U.S.C. §103

The Examiner rejected Claims 1, 4, 7, 8, 11 and 14 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,009,454 to Dummermuth, *et al.* ("Dummermuth"). Dummermuth discloses a multi-tasking operating system for real-time control of industrial processes. (Abstract). Multi-tasking is provided by recognizing that both ladder-type and state-type programs can be considered as simply a collection of individual instructions linked together by an

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implicit pointer list. At the conclusion of any instructions, a pointer may be developed to a single next instruction. (Column 2, lines 48-53).

Dummermuth, however, does not teach or suggest a context controller for managing multitasking in a processor that includes a background task controller that cyclicly activates a context corresponding to another background task when a number of instructions executed with respect to a given background equals a dynamically-programmable time slice value. (Claims 1 and 8). Instead, Dummermuth teaches a multi-tasking operation that "switches between tasks after a predetermined number of instructions by making the execution of each instruction explicit." (Column 7, lines 23-26). This differs from the present invention where a slice value is dynamically-programmable instead of predetermined. Since Dummermuth does not teach or suggest each and every element of independent Claims 1 and 8, the Examiner cannot establish a *prima facie* case of obviousness of Claims 1 and 8 and Claims dependent thereon. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 1, 4, 7, 8, 11 and 14 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

Furthermore, it would not have been obvious to one skilled in the art to arrive at managing multitasking in a processor as claimed in Claims 1 and 8 according to Dummermut's teaching. On the contrary, Dummermut teaches away from the multitasking managing of Claims 1 and 8 since Dummermuth teaches switching from one task to another task only after completing a predetermined number of instructions.

III. Rejection of Claims 2, 6, 9 and 13 under 35 U.S.C. §103

The Examiner rejected Claims 2, 6, 9 and 13 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of U.S. Patent No. 6,085,218 to Carmon. As discussed

above, Dummermuth does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Carmon does not cure the deficiencies of Dummermuth. Instead, Carmon is directed to monitoring a multi-task system by detecting overrun of any task beyond a declared maximum processor cycle limit for the task. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and Carmon does not cure the deficiencies of Dummermuth, then the Examiner cannot establish a case of obviousness of dependent Claims 2, 6, 9 and 13. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 2, 6, 9 and 13 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

IV.   Rejection of Claims 5 and 12 under 35 U.S.C. §103

The Examiner rejected Claims 5 and 12 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of U.S. Patent No. 5,528,513 to Vaitzblit, *et al.* ("Vaitzblit"). As discussed above, Dummermuth does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Vaitzblit does not cure the deficiencies of Dummermuth. Instead, Vaitzblit is directed to a scheduler that alternates between real-time tasks and general-purpose tasks using a weighted round-robin scheme. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and Vaitzblit does not cure the deficiencies of Dummermuth, then the Examiner cannot establish a case of obviousness of dependent Claims 5 and 12. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 5 and 12 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

V.   Rejection of Claims 3 and 10 under 35 U.S.C. §103

The Examiner rejected Claims 3 and 10 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of U.S. Patent No. 5,239,652 to Seibert, *et al.* ("Seibert"). As discussed above, Dummermuth does not teach or suggest each and every element of independent Claims 1 and 8. Furthermore, Seibert does not cure the deficiencies of Dummermuth. Instead, Seibert is directed to reducing the power consumption of a computer by determining when the central processing unit is not actively processing and generating a power-off signal to a control logic circuit. (Abstract). Since the Examiner did not establish a *prima facie* case of obviousness of independent Claims 1 and 8, and Seibert does not cure the deficiencies of Dummermuth, then the Examiner cannot establish a case of obviousness of dependent Claims 3 and 10. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 3 and 10 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

VI.   Rejection of Claims 15, 18 and 21-22 under 35 U.S.C. §103

The Examiner rejected Claims 15, 18 and 21-22 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of U.S. Patent No. 5,713,038 to Motomura. As discussed above with respect to independent Claims 1 and 8, Dummermuth does not teach or suggest switching between tasks using a dynamically-programmable time slice value as claimed in independent Claim 15. Furthermore, Motomura does not cure the deficiencies of Dummermuth. Instead, Motomura is directed to a microprocessor that has a register file which allows a higher speed, more flexible, context switching as compared to conventional microprocessors. (Column 3, lines 15-17).

Since Dummermuth does not teach each and every element of independent Claim 15 and Motomura does not cure its deficiencies, then the Examiner can not establish a *prima facie* case of obviousness of independent Claim 15 and Claims dependent thereon. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 15, 18 and 21-22 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims. Additionally, a person having ordinary skill in the art could not have arrived at the processor claimed in Claim 15 by combining the teachings of Dummermut and Motomura since neither Dummermut or Motomura teach or suggest switching between tasks using a dynamically-programmable time slice value.

VII.   Rejection of Claims 16, 17, 19 and 20 under 35 U.S.C. §103

The Examiner rejected Claim 17 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of Motomura and further in view of Seibert. The Examiner rejected Claim 19 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of Motomura and in further view of Vaitzblit. In addition, the Examiner rejected Claims 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over Dummermuth in view of Motomura and in further view of Carmon. As stated above, Dummermuth does not teach or suggest each and every element of independent Claim 15. Furthermore, as stated above with respect to previous rejections, neither Motomura, Seibert, Vaitzblit or Carmon cure the deficiencies of Dummermuth. No combination, therefore, of Motomura, Seibert, Vaitzblit, Carmon or Dummermuth teaches or suggests each and every element of Claims 16, 17, 19 and 20. The Examiner, nevertheless, cannot establish a *prima facie* case of obviousness with respect to Claims 16, 17, 19 and 20. Accordingly, the Applicants respectfully traverse the Examiner's rejection of Claims 16, 17, 19 and 20 under 35 U.S.C. §103(a) and request the Examiner withdraw the rejection with respect to these claims.

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V.   Conclusion

In view of the foregoing remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-22. Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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IN THE CLAIMS:

(1) Kindly amend Claim 1 as follows:

1.   (Amended) A context controller for managing multitasking <u>of a plurality of tasks</u> <u>including foreground tasks and background tasks</u> in a processor, comprising:

a time slice instruction counter that counts a number of instructions executed with respect to a given background task; and

a background task controller that cyclicly activates a context corresponding to another background task when said number equals a dynamically-programmable time slice value.

(2) Kindly amend Claim 8 as follows:

8.   (Amended) A method of managing multitasking <u>of a plurality of tasks including</u> <u>foreground tasks and background tasks</u> in a processor, comprising the steps of:

counting a number of instructions executed with respect to a given background task; and

cyclicly activating a context corresponding to another background task when said number equals a dynamically-programmable time slice value.

(3) Kindly amend Claim 15 as follows:

15. (Amended) A processor, comprising:

an instruction decoder that decodes instructions received into said processor and corresponding to a plurality of tasks <u>which includes foreground tasks and background tasks</u>;

a plurality of register sets, corresponding to said plurality of tasks, that contain operands to be manipulated;

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an execution core, coupled to said instruction decoder and said plurality of register sets, that executes instructions corresponding to an active one of said plurality of tasks to manipulate ones of said operands; and

a context controller, coupled to said instruction decoder and said execution core, that manages multitasking with respect to said plurality of tasks, including:

a time slice instruction counter that counts a number of instructions executed with respect to a given background task; and

a background task controller that cyclicly activates a context corresponding to another background task when said number equals a dynamically-programmable time slice value.